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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/071,373 | 02/08/2002 | Jason M. Howard | 884.584US1 | 1781 |

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| EXAMINER |
|---|
| DO, CHAT C |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2193 | |

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

| | Application No. | Applicant(s) |
|---|---|---|
| **Office Action Summary** | 10/071,373 | HOWARD ET AL. |
| | Examiner | Art Unit |
| | Chat C. Do | 2193 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☒ This action is **FINAL**.     2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)☒ Claim(s) *8-30* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

## Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

## DETAILED ACTION

1.      This communication is responsive to Amendment filed 07/14/2005.

2.      Claims 8-30 are pending in this application. Claims 8, 16, and 23 are independent

claims. In Amendment, claims 1-7 are cancelled. This Office Action is made final.

### *Claim Rejections - 35 USC § 102*

3.      The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.      Claims 8-9, 15-16, and 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by

Chip et al. ("The Coreware Methodology: building a 200 Mflop processor in 9 man months").

        Re claim 8, Chip et al. disclose in Figures 2 and 4 an integrated circuit (e.g.

Figure 4) comprising: a multiplier (e.g. FMUL in Figure 2) coupled to receive interleaved

operands and to produce a product (e.g. output of FMUL in Figure 2), and a multi-

threaded accumulator (e.g. FADD in Figure 2 and page 550 right column lines 8-12)

coupled to the multiplier to receive the product.

        Re claim 9, Chip et al. further disclose in Figures 2 and 4 a control circuit to

interleave input interleaved operands from different operand streams into the multiplier

(e.g. Opcode circuit in Figure 4).

Re claim 15, Chip et al. further disclose in Figures 2 and 4 the integrated circuit (e.g. Figure 4) is a circuit selected from the group comprising a processor (e.g. abstract), a memory (e.g. register files in Figure 4), a memory controller (e.g. Opcode control in Figure 4), an application specific integrated circuit, and a communications device (e.g. page 549 left column under graphic processor).

Re claim 16, Chip et al. disclose in Figures 2 and 4 an accumulator circuit (e.g. FADD in Figure 2) to accept operands from different threads interleaved in time (e.g. page 550 lines 9-13 right column), the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads (e.g. Figure 2 wherein the FADD holds 4 separate registers for xt, yt, zt, and wt respectively).

Re claim 19, Chip et al. further disclose in Figures 2 and 4 the operands are floating point numbers in IEEE single precision format (e.g. page 551 line 5 under conclusion section).

Re claim 20, Chip et al. further disclose in Figures 2 and 4 the operands are floating point numbers in a floating point format other than IEEE single precision format (e.g. page 551 line 5 under conclusion section).

Re claim 21, Chip et al. further disclose in Figures 2 and 4 the floating point numbers include exponent fields with a least significant bit weight other than one (e.g. page 550 lines 4-5 in right column).

Re claim 22, Chip et al. further disclose in Figures 2 and 4 the floating point numbers include exponent fields with a least significant bit weight equal to thirty-two (e.g. page 550 lines 4-5 in right column).

Re claim 23, Chip et al. disclose in Figures 2 and 4 a multiplier to produce a

product (e.g. output of FMUL as a*x in page 550); and an accumulator (e.g. FADD in

Figure 2) coupled to receive the product from the multiplier, the accumulator including

sequential elements to provide a multi-threaded capability (e.g. page 550 lines 9-14 right

column).

## Claim Rejections - 35 USC § 103

5.       The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

6.       Claims 10-11 are rejected under 35 U.S.C. 103(a) as being obvious over Chip et al. ("The

Coreware Methodology: building a 200 Mflop processor in 9 man months") in view of

Debabrata et al. ("A 600 MHz half-bit level pipelined accumulator-interleaved multiplier

accumulator core").

Re claim 10, Chip et al. disclose in Figures 2 and 4 the multi-threaded

accumulator is configured to sum floating point numbers having mantissas (e.g. FADD in

Figure 2). Chip et al. do not disclose the mantissa is in carry-save format. However,

Debabrata et al. disclose in Figure 4 the multi-threaded accumulator is configured to sum

floating point numbers having mantissas in carry-save format (e.g. Figure 4 and page 502

lines 2-5). Therefore, it would have been obvious to a person having ordinary skill in the

art at the time the invention is made to replace the mantissas in carry-save format as seen

in Debabrata et al.'s invention into Chip et al.'s invention because it would enable to

increase the system performance (e.g. page 502 last two lines and page 503 first two

lines).

Re claim 11, Chip et al. further disclose in Figures 2 and 4 the multi-threaded

accumulator includes at least one intermediate register to facilitate accumulating two

interleaved product streams simultaneously (e.g. FADD in Figure 2).

7.      Claims 12-14, 17-18, and 24-30 are rejected under 35 U.S.C. 103(a) as being obvious

over Chip et al. ("The Coreware Methodology: building a 200 Mflop processor in 9 man

months") in view of Choquette (U.S. 6,480,872).

Re claim 12, Chip et al. do not disclose in Figures 2 and 4 a floating point

conversion unit coupled between the multiplier and the multi-threaded accumulator to

convert the product from a first floating point representation to a second floating point

representation. However, Choquette discloses in Figure in Figure 4 a floating point

conversion unit coupled (e.g. 414) between the multiplier (e.g. 410 and 412) and the

multi-threaded accumulator (e.g. 416) to convert the product from a first floating point

representation to a second floating point representation (e.g. before the shifter and after

the shifter respectively).  Therefore, it would have been obvious to a person having

ordinary skill in the art at the time the invention is made to add a floating point

conversion unit coupled between the multiplier and the multi-threaded accumulator to

convert the product from a first floating point representation to a second floating point

representation as seen in Choquette's invention into Chip et al.'s invention because it

would enable to properly producing the correct product-accumulation by shifting or

aligning the product to the accumulation register (col. 5 lines 5-9).

Re claim 13, Chip et al. further disclose in Figures 2 and 4 the first floating point

representation includes an exponent field having a least significant bit weight of one, and

the second floating point representation includes an exponent field having a least

significant bit weight of thirty-two (e.g. page 550 lines 4-5 in right column).

Re claim 14, Chip et al. do not disclose in Figures 2 and 4 the multi-threaded

accumulator circuit includes at least one constant shifter to conditionally shift a mantissa

thirty-two bit positions. However, Choquette discloses in Figure 4 a constant shifter (e.g.

414) to conditionally shift a mantissa thirty-two bit positions. Therefore, it would have

been obvious to a person having ordinary skill in the art at the time the invention is made

to add a constant shifter for shifting a mantissa thirty-two bit positions as seen in

Choquette's invention into Chip et al.'s invention because it would enable to properly

producing the correct product-accumulation by shifting or aligning the product to the

accumulation register (col. 5 lines 5-9).

Re claims 17-18, Chip et al. do not disclose in Figures 2 and 4 a constant shifter

prior to a first intermediate register, and a multiplexor subsequent to the first intermediate

register and an adder circuit prior to a second intermediate register; and a second

multiplexor subsequent to the second intermediate register. However, Choquette

discloses in Figure 4 a constant shifter (414) prior to a first intermediate register (411),

and a multiplexor subsequent (e.g. mux prior selecting operands into adder 416 on the

left) to the first intermediate register and an adder circuit (e.g. 416) prior to a second

intermediate register; and a second multiplexor (e.g. mux prior selecting operands into

adder 416 on the right) subsequent to the second intermediate register (e.g. 418).

Therefore, it would have been obvious to a person having ordinary skill in the art at the

time the invention is made to add a constant shifter prior to a first intermediate register,

and a multiplexor subsequent to the first intermediate register and an adder circuit prior to

a second intermediate register; and a second multiplexor subsequent to the second

intermediate register as seen in Choquette's invention into Chip et al.'s invention because

it would enable to properly producing the correct product-accumulation by shifting or

aligning the product to the accumulation register (col. 5 lines 5-9).

Re claim 24, it has same limitations cited in claim 12. Thus, claim 24 is also

rejected under the same rationale as cited in the rejection of rejected claim 12.

Re claim 25, Chip et al. further disclose in Figures 2 and 4 the accumulator (e.g.

FADD in Figure 2) is configured to produce a present sum from the converted product

(e.g. output of FMUL) and a previous sum (e.g. feedback from FADD) having the second

exponent weight.

Re claim 26, Chip et al. do not disclose a post-normalization unit to convert the

present sum to a floating-point resultant having the first exponent weight. However,

Choquette discloses in Figure 4 a post-normalization unit to convert the present sum to a

floating-point resultant having the first exponent weight (e.g. feedback of register C into

the mux prior entering shifter 414 in Figure 4). Therefore, it would have been obvious to

a person having ordinary skill in the art at the time the invention is made to add a post-

normalization unit to convert the present sum to a floating-point resultant having the first

exponent weight as seen in Choquette's invention into Chip et al.'s invention because it would enable to properly provide a desire format as predetermined by the system.

Re claim 27, Chip et al. further disclose in Figures 2 and 4 the accumulator includes: an adder path (e.g. Figure 2). Chip et al. do not disclose an adder bypass path. However, Choquette discloses in Figure 4 an accumulator including an adder bypass path (e.g. output of 412 directly feeds to the result register 416). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a bypass path as seen Choquette's invention into Chip et al.'s invention because it would enable to increase the system performance by bypassing the alignment.

Re claim 28, it has same limitations cited in claim 21. Thus, claim 28 is also rejected under the same rationale as cited in the rejection of rejected claim 21.

Re claim 29, it has same limitations cited in claim 22. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 22.

Re claim 30, it has same limitations cited in claim 10. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

### *Response to Arguments*

8.      Applicant's arguments filed 07/14/2005 have been fully considered but they are not persuasive.

a.      The applicant argues in pages 7-9 for independent claims 8, 16, and 23 that the cited reference by Chip et al. fails to disclose the multiplier coupled to receive interleaved operands as cited in the claimed invention generally.

The examiner respectfully submits that cited reference by Chip et al. clearly show the multiplier coupled to receive interleaved operands as Chip et al. clearly shown in Figure 2 and terminology "interleaved" is used in discussing. As seen in Figure 2, multiple operands {x, y, z, w} and {a, b, e, d, ...m, n, o, p} are multiplex into the multiplier. The output of Figure 2 is seen or done in ¼ of the cycle time of table 1 (e.g. see page 550 first paragraph on the right column).

b.      The applicant argues in pages 9-10 for claims 10-11 that the Office Action for support of the combination of Chip et al. with Debabrata et al. are not found in the cited documents.

The examiner respectfully submits that the secondary reference by Debabrata et al. clearly disclose the lacking feature in the primary reference wherein the accumulator is performed in carry-save format. In Page 502, Debabrata et al. disclose the multiply-accumulator architecture comprising the accumulator performing in carry-save format and also the advantage of having the accumulator performing in carry-save format under section "Performance of the architecture: Carry-save Accumulation Bottleneck" in pages 502-503. Clearly, Debabrata et al. provide the support to combine with the primary reference by Chip et al. for its missing feature.

c.      The applicant argues in page 11 for claim 14 that there is no teaching or suggestion in the cited portion of cited references to combine the shifter of Choquette

with the matrix multiplication based on interleaved multiplier accumulator algorithm of

Chip et al.

> The examiner respectfully submits that the secondary reference by Choquette
>
> clearly disclose the scenario of using the shifter when the two operands is mis-
>
> alignment (e.g. col. 5 line 5-10).

d.      The applicant argues in page 11 for claim 27 that Office action fails to show how

the suggestion to make the claimed combination and the reasonable expectation of

success are found in the cited documents.

> The examiner respectfully submits that the obvious reason to have an adder
>
> bypass path is to bypass the adder which would yield less time or clock to
>
> produce the summation. Therefore, it would have been obvious to an ordinary
>
> skill in the art at the time the invention is made to have a bypass path in order to
>
> increase the system performance.

### *Conclusion*

9.      The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

e.      U.S. Patent No. 6,438,569 to Abbott discloses a sum of production datapath.

f.      U.S. Patent No. 5,847,981 to Kelley et al. disclose a multiply and accumulate

circuit.

g.      U.S. Non-Patent Literature to Debabrata et al. disclose an architectural synthesis

of performance-driven multipliers with accumulator interleaving.

10.     **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The

examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

September 12, 2005

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